Docket No. ROC920030054US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	GERALD G. FAGERNESS ET AL.
Serial No.	:	10/625,954
Filed	:	July 24, 2003
For	:	METHODS AND APPARATUS FOR INDEXING MEMORY OF A NETWORK PROCESSOR
Examiner	:	ROBERT C. SCHEIBEL
Group Art Unit	:	2616

APPEAL BRIEF UNDER 37 CFR § 41.37

Commissioner for Patents
Board of Patent Appeals and Interferences
United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Notice of Appeal filed in this application on February 28, 2008, Applicants hereby submit Appellants' Brief and a petition for a one-month extension of time together with the requisite fees set forth in 37 CFR § 1.17, thus extending the due date for Appellants' Brief to May 28, 2008.

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I. Real Party in Interest (37 CFR §41.37(c)(1)(i))

The real party in interest is IBM Corporation, the assignee of the subject application.

II. Related Appeals and Interferences (37 CFR §41.37(c)(1)(ii))

The applicant and the undersigned representative are not aware of any other appeals or interferences that will directly affect or be directly affected by, or have a bearing on, the Board's decision in the pending appeal.

III. Status of Claims (37 CFR §41.37(c)(1)(iii))

Claims 1-19 were originally filed in the application. Claims 1, 11, 16, and 18 are independent claims, and claims 2-10, 12-15, 17, and 19 are dependent claims.

Claims 1-19 stand finally rejected, and are the subject of this appeal.

IV. Status of Amendments (37 CFR §41.37(c)(1)(iv))

Applicants filed an Amendment After Final Rejection on January 22, 2008. In that Paper, Applicants proposed an amendment to claim 11 to improve its idiomatic English form.

In an Advisory Action mailed February 19, 2008, the Office indicated that the amendment to claim 11 would be entered for purposes of appeal and that the rejection of the claims would be sustained.

V. Summary of Claimed Subject Matter (37 CFR §41.37(c)(1)(v))

Pursuant to 37 C.F.R. §1.192(c)(5), the following are statements of the claimed subject matter.

Independent claim 1 recites: "1. A method for determining a control block index for a data cell received by a network processor coupled to an ATM network (page 13, lines 23-30; FIG. 4) comprising: receiving a data cell at a port, the data cell having a virtual path identifier and a virtual channel identifier (page 13, lines 28-32; item 402 of FIG. 4); determining a port number for the port (page 13, line 32 - page 14, line 2; item 403 of FIG. 4); employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create a first address(page 14, lines 3-10; item 404 of FIG. 4); employing the first address to access a first memory and to obtain a first entry from the first memory (page 14, lines 10-15; item 405 of FIG. 4), the first entry specifying: a first base memory address; a number of bits of the port number to use in the control block index; a number of bits of the virtual path identifier to use in the control block index; and a number of bits of the virtual channel identifier to use in the control block index (page 8, lines 19 - page 20 line 18; page 11, lines 4-21; page 11, line 22 - page 12, line 4; page 9, lines 6-18; items 214, 216, 218, and 220 of FIGS. 2 and 3); and employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create the control block index for the data cell (page 14, lines 16-25; item 406 of FIG. 4).

Independent claim 11 recites: "11. A system adapted to determine a control block index for each data cell received by a network processor coupled to an ATM network (page 4, lines 28-30; FIG. 1) comprising: a first memory (item 110 of FIG. 1) having a plurality of entries (page 5, lines 10-18), each entry including: a base memory address; a number of bits of a port number of a port that receives a data cell to use in the control block index; a number of bits of a virtual path identifier of the data cell to use in the control block

index; and a number of bits of a virtual channel identifier of the data cell to use in the control block index (page 8, lines 19 – page 20, line 18; page 11, lines 4-21; page 11, line 22 – page 12, line 4; page 9, lines 6-18; items 214, 216, 218, and 220 of FIGS. 2 and 3); and a logic circuit (item 112 of FIG. 112) adapted to: generate an address for accessing the first memory based on bits of at least one of a port number of a port that receives a first data cell, a virtual path identifier for the first data cell and a virtual channel identifier for the first data cell; employ the address to obtain an entry of the first memory; and employ the base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the entry to create a control block index for the first data cell (page 6, lines 27-page 7, line 5)."

Independent claim 16 recites: "16. A method for address mapping in a network processor, the method comprising: determining a port number of a port that receives a data cell (page 13, line 32 – page 14, line 2; item 403 of FIG. 4); determining a virtual path identifier and a virtual channel identifier for the data cell (page 14, lines line 3 – 12); creating a first index based on at least one of the port number, the virtual path identifier and the virtual channel identifier (page 14, lines 3-5); accessing one of a plurality of entries stored in a first on-chip memory using the first index (page 14, lines 10 -15); creating a second index based on the accessed entry of the first on-chip memory (page 14, lines 16 – 25); and accessing an entry of a second memory based on the second index (page 6, line 27 – page 7, line 5)."

Independent claim 18 recites: "18. A system adapted to perform address mapping in a network processor comprising: a first on-chip memory (item 110 of FIG. 1) having a plurality of entries; and a logic circuit (112 of FIG. 1) adapted to: create a first index based on at least one of a number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell; access one of the plurality of entries stored in the first on-chip memory using the first index (page 6,

lines 7 - 30; page 14, lines 3-15; FIGS. 1 and 2); and create a second index based on the accessed entry of the first on-chip memory(page 6, line 33 - page 7, line 5; page 14, lines 16 - 25)."

None of the claims contain an element expressed as a "means for" or "step for" performing a specified function without the recital of structure, material, or acts in support thereof.

VI. Grounds Of Rejection To Be Reviewed On Appeal (37 CFR §41.37(c)(1)(vi))

The grounds of rejection for review are:

(A) the rejection of independent claims 1 and 11 under 35 U.S.C. § 103 as being obvious over the combination of U.S. Patent 5,414,701 to *Shtayer et al.* (hereinafter "*Shtayer et al.*") and U.S. Patent No. 6,356,552 to *Foglar* (hereinafter "*Foglar*"); and

(B) the rejection of independent claims 16 and 18 under 35 U.S.C. § 102 as being anticipated by *Shtayer et al.*

VII. Argument Of Each Ground Of Rejection Presented For Review (37 CFR §41.37(c)(1)(vii)))

A. The Rejection of independent claims 1 and 11 under 35 U.S.C. §103(a) should be reversed because it is based on an erroneous application of the secondary citation to *Foglar* and the asserted combination is deficient

Independent claim 1 recites features of a method that includes, *inter alia*,

determining a port number for a port,

employing bits of at least one of a virtual path identifier, a virtual channel identifier and the port number to create a first address, and …

employing a first base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by a first entry [of a first memory at the first address] to create a control block index for the data cell.

Independent claim 11 recites similar features in apparatus form.

This number of bits identifies a port that received data by specifying the number of bits of that port. (Application, page 11, lines 22 - 25; page 13 line 32 - page 14, line 1).

Applicants submit that the asserted combination fails to disclose at least the aforementioned claim features.

The Office has repeatedly conceded that *Shtayer et al.* does not teach or suggest that an alleged first entry specifies a number of bits of the port number to use in the control block index. (*Final Office Action*, page 6, first full paragraph). The Office nonetheless rejected claims 1 and 11 contending that *Foglar* provides the necessary disclosure of these features. (*Final Office Action*, pages 6 - 7).

Applicants do not agree that *Foglar* provides this necessary disclosure and assert that the Office is mischaracterizing the content of *Foglar*.

Specifically, the Office has characterized a value P discussed in *Foglar* as "a number of bits of the port number." (*Final Office Action*, page 6). A review of *Foglar*, including the portions of

Foglar cited by the Examiner, reveals that P is expressly defined to mean something else, however.

Foglar relates to a method by which sets of values representing various parameters can be allocated to addresses and discusses generating logical channel identifier (LCI) from portions of the following three parameters:

(i) a virtual path identifier (VPI);

(ii) a virtual channel identifier (VCI; and

(iii) a physical port number (PN).

Specifically, *Foglar* teaches that the PN value is shortened to P bits, which value "P" is expressly defined by *Foglar* to represent "the number of lines or termination units … with which an ATM unit is connected. (*Foglar*, Col. 7, lines 15-38).

In view of these express teachings, the P bits to which *Foglar* refers is, at best, arguably a number of ports (i.e., a sum of the connected ports). Indeed, the Office Action itself expressly describes P as "clearly the number of ports used in the creation of the LCI." (*Office Action*, page 3, last sentence of item #3)).

In contrast, the aforementioned features of claims 1 and 11 recite "a number of bits of a port number." This number, as explained at page 11, line 22 and page 13, line 32 of the present application, is usable to determine a port that received a data cell. This cannot reasonably be said to be the same as a number of ports used to do something. Stated another way, a number of connected ports (P of *Foglar*) is not the same as the claimed a number of bits of a port number, which need not be the same as the number of connected ports.

Thus, *Foglar* cannot remedy the acknowledged deficiency of *Shtayer et al.*

Accordingly, the rejection of independent claims 1 and 11 under 35 U.S.C. § 103 should be reversed.

B. Rejection of independent claims 16 and 18 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,414,701 to *Shtayer et al.* should be reversed because it is based on an erroneous interpretation of *Shtayer et al.*

Independent claim 16 recites a method including, *inter alia*, accessing one of a plurality of entries stored in a first on-chip memory using the first index.

Independent claim 18 recites a system that includes, *inter alia*, a first on-chip memory having a plurality of entries.

The Examiner contends that a link table illustrated in FIGS. 3 and 5 of *Shtayer et al.* are a plurality of entries and that notations of "internal – 16 entries" concerning the link table in FIGS. 2, 3, and 5 of that patent "clearly indicates that that the link table is internal." (*Final Office Action*, page 2).

Applicants acknowledge the presence of the notation "internal" in FIGS. 2, 3, and 5 of *Shtayer et al.* Applicants also acknowledge that anticipatory teaching may come from patent drawings. Nonetheless, Applicants respectfully submit that the Office's interpretation of this patent is incorrect because it is contrary to how one of ordinary skill in the art would interpret the notation "internal."

Firstly, no portion of *Shtayer et al.* connects these notations with a **location** of the link table (i.e., on chip or off). The absence of such a teaching is not surprising since the notation internal is an indication of the 16 entries in the table (i.e., there are 16 internal links). Indeed, a review of cited FIG. 2 of *Shtayer et al.* buttresses this interpretation, as it illustrates a data compression structure using the 16 links of the link table.

Secondly, when taken in context with the written description of *Shtayer et al.*, the presence of the notation "internal" does not indicate a location of the link table. Rather, the notation "internal" indicates that there are 16 entries in the link table itself. This is how one of ordinary skill would interpret this art. And, a review of the portions of *Shtayer et al.* describing these figures buttresses this conclusion. In describing FIG. 2, for

example, *Shtayer et al.* teaches "FIG. 2 illustrates a link table which has sixteen entries …." (*Shtayer et al.*, Col. 4, lines 42-43).

Stated another way, the Office's interpretation of *Shtayer et al.* is incorrect because it is at best unsupported and actually contradicts the teachings of that patent as a whole, which teachings provide an accurate meaning of the notation "internal."

In the Advisory Action, the Examiner contends that VP and VC tables of FIG. 2 are stored internally on a chip and do not have any "internal" notation. Thus, *Shtayer et al.* is "clearly trying to the relatively small link table from the other tables" and it is clear that the notation "internal" indicates that is stored on-chip "as opposed to external memory on which the other entries are stored." (*Advisory Action*, continuation of 11, first paragraph).

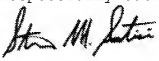
This position, however, fails to account for what FIG. 2 is disclosing. In that figure, the patent is disclosing an exemplary number of links in an exemplary link table and how each entry links to a VP table. For this reason, *Shtayer et al.* has no reason to make use of "internal" notations regarding the VP and VC tables to which the respective internal entries of the link table point. Stated another way, the absence of notations of "internal" is the result of the subject matter being illustrated, --namely the structure of the link table and a compression structure for data. Thus, the Examiner's late supplemental argument fails.

Accordingly, favorable reconsideration and withdrawal of the rejection claims 16-18 under 35 U.S.C. § 102 are respectfully requested.

VIII. Conclusion

In view of the law and facts stated herein, the Appellant respectfully submits that the rejections of the independent claims (claims 1, 11, 16, and 18) are deficient as a matter of law and should thus be reversed. Accordingly, Reversal of the rejections in this appeal is respectfully requested.

Respectfully Submitted,



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IX. Claims Appendix (37 CFR § 41.37(c)(1)(viii))

Claim 1. (Previously Presented) A method for determining a control block index for a data cell received by a network processor coupled to an ATM network comprising:

receiving a data cell at a port, the data cell having a virtual path identifier and a virtual channel identifier;

determining a port number for the port;

employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create a first address;

employing the first address to access a first memory and to obtain a first entry from the first memory, the first entry specifying:

a first base memory address;

a number of bits of the port number to use in the control block index; a number of bits of the virtual path identifier to use in the control block index; and

a number of bits of the virtual channel identifier to use in the control block index; and

employing the first base memory address and the number of bits of the port number, virtual path identifier-and virtual channel identifier specified by the first entry to create the control block index for the data cell.

Claim 2. (Original) The method of claim 1 wherein employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create the first address comprises employing bits of at least one of the virtual path identifier and the port number to create the first address.

Claim 3. (Original) The method of claim 1 wherein the first memory is an on-chip memory of the network processor.

Claim 4. (Original) The method of claim 3 wherein the first memory comprises an on-chip random access memory.

Claim 5. (Original) The method of claim 1 wherein employing the first base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the first entry to create the control block index for the data cell comprises:

selecting the number of bits of the port number specified by the first entry;

selecting the number of bits of the virtual path identifier specified by the first entry;

selecting the number of bits of the virtual channel identifier specified by the first entry;

catenating any selected bits; and

adding the catenated selected bits to the first base memory address.

Claim 6. (Original) The method of claim 5 further comprising:

shifting the control block index; and

adding the shifted control block index to a main system memory base offset so as to generate a control block memory address.

Claim 7. (Original) The method of claim 6 further comprising employing the control block memory address to obtain a control block from a main system memory.

Claim 8. (Original) The method of claim 5 further comprising verifying that non-selected port number, virtual path identifier and virtual channel identifier bits are zeroed.

Claim 9. (Original) The method of claim 1 further comprising pre-selecting which bits are used to form the first address.

Claim 10. (Original) The method of claim 1 further comprising selecting each entry for the first memory.

Claim 11. (Previously Presented) A system adapted to determine a control block index for each data cell received by a network processor coupled to an ATM network comprising:

a first memory having a plurality of entries, each entry including:

a base memory address;

a number of bits of a port number of a port that receives a data cell to use in the control block index;

a number of bits of a virtual path identifier of the data cell to use in the control block index; and

a number of bits of a virtual channel identifier of the data cell to use in the control block index; and

a logic circuit adapted to:

generate an address for accessing the first memory based on bits of at least one of a port number of a port that receives a first data cell, a virtual path identifier for the first data cell and a virtual channel identifier for the first data cell;

employ the address to obtain an entry of the first memory; and

employ the base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the entry to create a control block index for the first data cell.

Claim 12. (Original) The system of claim 11 wherein the first memory is an on-chip memory of the network processor.

Claim 13. (Original) The system of claim 11 wherein the logic circuit is adapted to create the control block index for the first data cell by:

selecting the number of bits of the port number specified by the entry of the first memory;

selecting the number of bits of the virtual path identifier specified by the entry; selecting the number of bits of the virtual channel identifier specified by the entry;

catenating any selected bits; and

adding the catenated selected bits to the base memory address specified by the entry to form the control block index.

Claim 14. (Original) The system of claim 13 wherein the logic circuit is further adapted to:

shift the control block index; and

add the shifted control block index to a main system memory base offset so as to generate a control block memory address.

Claim 15. (Original) The system of claim 11 further comprising a processor coupled to the first memory and the logic circuit and adapted to:

determine each entry within the first memory; and

determine which bits of a port number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell are employed to generate an address for the first memory.

Claim 16. (Original) A method for address mapping in a network processor, the method comprising:

determining a port number of a port that receives a data cell;

determining a virtual path identifier and a virtual channel identifier for the data cell;

creating a first index based on at least one of the port number, the virtual path identifier and the virtual channel identifier;

accessing one of a plurality of entries stored in a first on-chip memory using the first index;

creating a second index based on the accessed entry of the first on-chip memory; and

accessing an entry of a second memory based on the second index.

Claim 17. (Original) The method of claim 16 wherein each entry stored in the first on-chip memory contains a base address field and one or more of a number of port number bits field, a number of virtual path identifier bits field and a number of virtual channel identifier bits field.

Claim 18. (Original) A system adapted to perform address mapping in a network processor comprising:

a first on-chip memory having a plurality of entries; and

a logic circuit adapted to:

create a first index based on at least one of a number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell; access one of the plurality of entries stored in the first on-chip memory using the first index; and

create a second index based on the accessed entry of the first on-chip memory.

Claim 19. (Original) The system of claim 18 wherein each entry of the first on-chip memory contains a base address field and one or more of a number of port number bits field, a number of virtual path identifier bits field and a number of virtual channel identifier bits field.

X. Evidence Appendix

Not applicable.

XI. Related Proceedings Appendix

Not applicable.